REMARKS

The Applicant thanks the Examiner for the thorough examination of the application. No new matter is believed to be added to the application by this Amendment.

Entry Of Amendment

Entry of this Amendment under 37 C.F.R. 1.116 is respectfully requested because it cancels claims, thereby placing the application in condition for allowance. Alternately, entry is requested because it reduces issues for appeal.

Status of the Claims

Upon entry of this Amendment, claims 1, 3-16 and 19-20 are pending in the application. Claims 2, 17 and 18 are cancelled by this Amendment. The amendments to claims 1 and 11 find support in cancelled claims 2, 17 and 18. Claims 19 and 20 have been added to cover additional aspects of the invention.

Rejections Under 35 U.S.C. §103(a) Based On Nakano

Claims 1, 5, 11 and 16 are rejected under 35 U.S.C. §103(a) as being obvious over Nakano (U.S. Patent 6,529,181). Claims 3, 4,7-9, 12-15, 17 and 18 are rejected under 35 U.S.C. §103(a) as being obvious over Nakano in view of Uchino (U.S. Patent 6,040,816). The Examiner adds the teachings of Itakura (U.S. Patent 5,252,957) to Nakano (as applied to claim 1) reject claims 2, 6 and 10 under 35 U.S.C. §103(a) as being obvious. Applicant traverses.

The Present Invention and its Advantages

The present invention pertains to a novel LCD device that reduces power consumption and increases display quality by minimizing EMI (electromagnetic interference). One of the many novel features of the claimed invention resides in that at least two data buses are connected between the timing controller and respective source drivers. The inventive LCD device also utilizes a synchronized data sampling technology and timing controller configuration that minimizes the use of unnecessary voltage, thereby decreasing power consumption. In another aspect of the invention, the source driver separately samples the digital R/G/B data so that the power consumption is reduced. Another of the novel features of the invention includes having the number of data buses being in proportion to the number of clock signals output from the timing controller.

The present invention finds a typical embodiment in instantly amended claim 1, which sets forth:

> 1. An LCD device, comprising:
> a LCD panel;
> a plurality of source drivers applying data signals to the LCD panel;
> a plurality of gate drivers applying gate driving signals to the LCD panel;
> a timing controller outputting to the source drivers at least two clock signals having different phases, the timing controller separately outputting R/G/B data synchronized with each output signal to the source drivers; and
> at least two data buses transmitting the data separately output from the timing controller to the source drivers,
> wherein the at least two data buses are connected between the timing controller and the respective source drivers, a number of the data buses are in proportion to a number of clock signals output from

> the timing controller, and the source drivers separately sample the data to thereby reduce electricity consumption.

As shown in Figure 4, source drivers 43 apply data signals to the LCD panel 41, and the gate driver 45 applies gate-driving signals to the LCD panel 41. The timing controller 47 receives a data clock signal DCLK and R/G/B digital data, and outputs first and second clock signals CLK1 and CLK2 having different phases and various control signals to control the source and gate drivers 43 and 45. The timing controller 47 connects to each source driver by at least two data buses (see also Figure 6), where a first data bus DB1 transmits the digital data synchronized with the first clock signal CLK1 to each source driver 43, and a second data bus DB2 transmits the digital data synchronized with the second clock signal CLK2 to each source driver 43.

The advantages of using at least two data buses is described at paragraph 0053 of the specification:

> [0053] The timing controller 47 synchronizes digital data received from the system and synchronized with two clock signals through two data buses, and then separately outputs the synchronized digital data to the source drivers. As a result, electricity used in outputting the data can be reduced.

The advantages offered by the separate outputting of the timing controller 47 and the separate sampling of the source drivers 43 is explained in paragraph 0054 of the specification:

> [0054] The timing controller 47 separately outputs the digital data, so that the source driver 43 separately samples the digital data. Therefore, electricity used in sampling the digital data in the source

> driver 43 can be reduced, thereby substantially reducing electricity for driving the whole circuit as compared to the related art.

The advantages of the relationship between the timing controller 47 and the source drivers 43 are also explained in paragraphs 0063 (which utilizes three data buses) and 0064 of the specification:

> [0063] That is, the timing controller 47 separately outputs digital data received from the system and synchronized with the three clock signals per the R/G/B digital data through the three data buses to each source driver, thereby reducing the electric power used in outputting the data.
>
> [0064] Also, the timing controller 47 separately outputs digital data according to the R/G/B digital data, so that the source driver 43 separately samples the digital data according to the R/G/B digital data. Therefore, the electric power consumption for driving the whole circuit can be reduced.

Distinctions of the Invention over Nakano, Uchino and Itakura

Distinctions of the invention over the prior art have been place before the Examiner. For brevity, these distinctions are not repeated in full here.

Nakano pertains to a liquid crystal display apparatus having a display control unit to lower the clock frequency for driving pixels. Figure 1 of Nakano shows an LCD panel 10, drain drivers 130, gate drivers 140 and an interface unit 100 having a display control unit 110 and a power supply circuit 120. The circuit driving by Nakano is described at column 6, lines 22-43:

> The display control circuit 110 is formed of a single semiconductor integrated circuit (LSI) for controlling and driving the drain drivers 130 and the gate drivers 140 based on the display control signals including the clock signal CK, the display timing signal DTMG, the horizontal synchronization signal Hsync and the vertical

> synchronization signal Vsync, and the display data (R, G, B), all of which are transmitted thereto from the computer side.
>
> In this case, the display control unit 110 generates from the clock signal CK from the computer side, a first clock signal D4 (hereinafter referred to as the "clock signal D4") as a clock signal for latching display data, and a second clock signal D5 (hereinafter referred to as the clock signal D5") having the same frequency as and a different phase from the first clock signal D4. In this embodiment, the clock signal D5 is an inverted version of the clock signal D4.
>
> The clock signal D4 is transmitted to a group A of drain drivers 130 (odd-numbered drain drivers 130 in FIG. 1) through a signal line 131. The clock signal D5 in turn is transmitted to a group B of drain drivers 130 (even-numbered drain drivers 130 in FIG. 1) through a signal line 132.
>
> In response, the display control unit 110 reorders originally ordered display data received from the computer side, and outputs the reordered display data to the drain drivers 130 through a display data bus line 134.

Nakano, that is, fails to disclose or suggest separate outputting and sampling where "the timing controller separately outputting R/G/B data synchronized with each output signal to the source drivers" and "the source drivers separately sample the data to thereby reduce electricity consumption." (claims 1 and 11).

The Examiner then turns to Uchino for teachings pertaining data synchronized with a rising edge time and falling edge time of each clock signal. However, Uchino fails to address the deficiencies of Nakano in teaching or suggesting separate outputting and sampling as set forth in claims 1 and 11.

The Examiner turns to Itakura for teachings pertaining to the number of data busses in proportion to the number of clock signals. However, Itakura fails to address the deficiencies of Nakano in teaching or suggesting separate outputting and sampling as set forth in claims 1 and 11.

In her Response to Arguments at page 7 of the Office Action, the Examiner asserts: "As to the separate sampling to reduce energy consumption, this argument is directed towards unclaimed subject matter." However, claim 1 clearly sets forth that "the source drivers separately sample the data to thereby reduce electricity consumption." (see also claim 11).

Therefore, one having ordinary skill would not be motivated by Nakano, Uchino and Itakura (alone or in combination) to produce the present invention embodied in claims 1 and 11. A *prima facie* case of obviousness has not been made. Claims depending upon claims 1 and 11 are patentable for at least the above reasons.

These rejections are overcome and withdrawal thereof is respectfully requested.

As the Examiner will note, claims 19 and 20 have been added to the present application to cover additional aspects of the present invention.

Prior Art Cited But Not Utilized By The Examiner

The prior art cited but not utilized by the Examiner shows the status of the conventional art that the invention supercedes. No additional remarks are accordingly necessary.

The Drawings

The Examiner has found the drawing figures to be acceptable in the Office Action mailed March 22, 2004.

Priority

The Examiner has acknowledged priority most recently in the Office Action Summary of the Office Action mailed March 22, 2004.

Assignment

The assignment was recorded on December 28, 2001 at reel 012420, frames 0478-0480

Conclusion

The Examiner's rejections have been overcome, obviated or rendered moot. No issues remain. The Examiner is accordingly respectfully requested to place the application in condition for allowance and to issue a Notice of Allowability.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert E.

Goozner (Reg. No. 42,593) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

Date: November 9, 2005

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